REMARKS

The Office Action of November 29, 2006, has been received and reviewed.

Claims 1-3, 5-41, and 43-55 are currently pending and under consideration in the above-referenced application. Each of claims 1-3, 5-41, and 43-55 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections under 35 U.S.C. § 103(a)

Claims 1-3, 5-41, and 43-55 stand rejected under 35 U.S.C. § 103(a).

Lin in View of Horiuchi

Claims 1-3, 5-9, 19, 21, 22, 30-35, 43, 44, and 50-52 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent 5,258,648 to Lin (hereinafter "Lin"), in view of teachings from U.S. Patent 6,297,553 to Horiuchi et al. (hereinafter "Horiuchi").

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Lin teaches a composite flip chip semiconductor device 10 including a semiconductor die 12 with solder balls 16 formed on bonding pads 14. Col. 4, lines 20-24. The active surface of the semiconductor die 12 is coupled to an interposer 22 with conductive vias 24 by aligning the solder bumps 16 and conductive vias 24. FIG. 1; col. 4, lines 51-55. Conductive traces 26 on

the surface of the interposer 22 coupled to the active surface of the semiconductor die 12 electrically connect solder balls 16 to vias 24. FIG. 5; col. 4, lines 58-68.

Horiuchi teaches a semiconductor chip 10 electrically connected to an interposing substrate 12 through connection bumps 14. Col. 4, lines 35-38. The interposing substrate 12 is formed from an insulating material and includes wiring patterns 24/30 formed on opposing surfaces. FIG. 2, col. 4, lines 62-27. The wiring pattern 24 on one surface of the interposing substrate 12 is electrically connected to the wiring pattern 30 on the other surface through vias that include metal plating. FIG. 2, col. 5, lines 16-31.

It is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 1-3, 5-9, 19, 21, 22, 30-35, 43, 44, and 50-52.

Independent claim 1, as amended herein, recites a chip-scale package that includes a semiconductor device, an interposer with a first surface disposed adjacent an active surface of the semiconductor device and at least one electrically conductive bump. Solder forms at least one electrically conductive via and a conductive structure that protrudes from a first surface of the interposer. The electrically conductive via extends at least partially through the substrate to communicate with a corresponding bond pad of the semiconductor device. The substrate also includes a second surface, which is opposite from the first surface, which carries at least one conductive trace, which communicates with the at least one conductive via.

It is respectfully submitted that neither Lin nor Horiuchi, alone or in combination, teaches or suggests a chip-scale package that includes an interposer with solder forming at least one protruding conductive structure and a corresponding electrically conductive via. Rather, Lin teaches a flip chip device with solder balls 32 positioned beneath and secured to each via 24 and coupled to a substrate 34. *See* Lin, col. 5, lines 23-25. As shown in Figure 3, the solder balls 32 of Lin are not continuous with the vias 24. *Id.*, FIG. 3.

Horiuchi also lacks any teaching or suggestion that the interposer may include solder forming a protruding conductive structure and a corresponding electrically conductive via. Specifically, Horiuchi teaches external connection terminals 26 that are separated from the vias 24 by terminal lands 28.

As Lin and Horiuchi do not teach or suggest each and every element of independent claim 1, it is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1. Therefore, under 35 U.S.C. § 103(a), the subject matter to which independent claim 1 is directed is allowable over the subject matter taught in Lin and Horiuchi.

Claims 2, 3, 5-9, and 19 are each allowable, among other reasons, for depending directly from claim 1, which is allowable.

Independent claim 21, as amended herein, is directed to a chip-scale package with an interposer that includes first and second surfaces, solder forming conductive vias and conductive structures protruding from the conductive vias. The conductive vias extend through the interposer. In addition, the package of independent claim 21 includes a semiconductor device invertedly disposed adjacent to the first surface of the interposer. The first surface of the substrate includes contact areas that correspond to an arrangement of bond pads on the semiconductor device. An opposite, second surface of the substrate, which faces away from the semiconductor device, carries at least one conductive trace.

The combination of Lin and Horiuchi does not teach or suggest a chip-scale package with solder that forms at least one protruding conductive structure and a corresponding conductive via, as explained herein with respect to claim 1.

As Lin and Horiuchi do not teach or suggest each and every element of independent claim 21, it is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 21. Therefore, under 35 U.S.C. § 103(a), the subject matter to which independent claim 21 is directed is allowable over the subject matter taught in Lin and Horiuchi.

Claims 22, and 30-35 are each allowable, among other reasons, for depending directly from claim 21, which is allowable.

Independent claim 43, as amended herein, recites a carrier with solder forming at least one via and a conductive structure protruding from the at least one via. The conductive structures protrudes from a first surface of the carrier, adjacent to which a semiconductor device is to be positioned. The via extends between the first surface of the carrier and an opposite,

second surface. At least one conductive trace, which extends laterally from an end of the via, is carried by the second surface of the carrier.

The combination of Lin and Horiuchi does not teach or suggest a carrier with solder forming at least one protruding conductive structure and a corresponding via, as described herein with respect to claim 1.

As Lin and Horiuchi do not teach or suggest each and every element of independent claim 43, it is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 43. Therefore, under 35 U.S.C. § 103(a), the subject matter to which independent claim 43 is directed is allowable over the subject matter taught in Lin and Horiuchi.

Claims 44, 50-52 are each allowable, among other reasons, for depending directly from claim 43, which is allowable.

Lin and Horiuchi View of Gnadinger

Claims 11-14, 20, 23-25, 37-41, and 45-49 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Lin and Horiuchi as applied to claims 1, 21 and 43 above, and further in view of U.S. Patent 5,229,647 to Gnadinger (hereinafter "Gnadinger").

Claims 11-14, and 20 are each allowable, among other reasons, as depending either directly or indirectly from independent claim 1, which is allowable.

Claims 23-25 and 37-41 are each allowable, among other reasons, as depending either directly or indirectly from independent claim 21, which is allowable.

Claims 45-49 are each allowable, among other reasons, as depending either directly or indirectly from independent claim 43, which is allowable.

Lin in View of Kim

Claims 10, 15, 18, 26, 27 and 36 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Lin and Horiuchi as applied to

claims 1 and 21 above, and further in view of U.S. Patent 6,004,867 to Kim et al. (hereinafter "Kim").

Each of claims 10, 15, and 18 are allowable, among other reasons, as depending directly or indirectly from independent claim 1, which is allowable.

Each of claims 26, 27, and 36 are allowable, among other reasons, as depending directly or indirectly from independent claim 43, which is allowable.

Lin in View of Higgins

Claims 16, 17, 28 and 29 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Lin and Horiuchi as applied to claims 1, 15 and 21 above, and further in view of U.S. Patent 6,004,867 to Kim and U.S. Patent 6,294,405 to Higgins, III (hereinafter "Higgins").

Claims 16 and 17 are each allowable, among other reasons, as depending indirectly from independent claim 1, which is allowable.

Claims 28 and 29 are each allowable, among other reasons, as depending indirectly from independent claim 21, which is allowable.

Lin in View of Tokuda

Claims 53 through 55 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Lin and Horiuchi as applied to claim 43 above, and further in view of U.S. Patent 5,870,289 to Tokuda et al. (hereinafter "Tokuda").

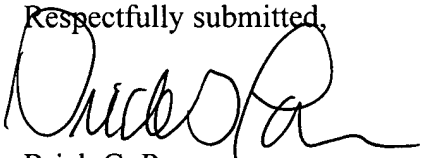
Each of claims 53-55 is allowable, among other reasons, as depending directly or indirectly from independent claim 43, which is allowable.

Withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1-3, 5-41, and 43-55 is respectfully requested, as is allowance of each of these claims.

CONCLUSION

It is respectfully submitted that each of claims 1-3, 5-41, and 43-55 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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